TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. END920010024US1

In Re Application Of: **Carpenter et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/924,204	8/7/2001	Chang, Rick Kiltae	3729

Invention: **COUPLING OF CONDUCTIVE VIAS TO COMPLEX POWER-SIGNAL SUBSTRUCTURES**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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IFW AF/3729

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Carpenter *et al.*

Art Unit: 3729

Serial No.: 09/924,204

Dkt. No.: END920010024US1

Filed: 8/7/2001

Examiner: Chang, Rick Kiltae

Title **COUPLING OF CONDUCTIVE VIAS TO COMPLEX POWER-SIGNAL SUBSTRUCTURES**

Commissioner for Patents
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BRIEF OF APPELLANT

This Appeal Brief, pursuant to the Notice of Appeal filed March 31, 2004, is an appeal from the rejection of the Examiner dated December 31, 2003.

REAL PARTY IN INTEREST

International Business Machines, Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 28-31, 33, 35-44, 49, 51-54, 56 and 58-64 are currently pending. Claims 28-31,

33, 35-44, 49, 51-54, 56 and 58-64 have been rejected. This Brief is in support of an appeal from the rejection of claims 28-31, 33, 35-44, 49, 51-54, 56 and 58-64.

STATUS OF AMENDMENTS

There are no After-Final Amendments which have not been entered.

SUMMARY OF INVENTION

All features of the following summary of the invention are shown in FIG. 6 in conjunction with the description of FIG. 6 on page 12, lines 1-18.

The present invention discloses an electrical structure, comprising: a complex power-signal (CPS) substructure, a dielectric-metallic (DM) laminate, and a first multilevel conductive via through the DM laminate. The CPS substructure may have passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance. The DM laminate includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2. The first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure. The first multilevel conductive via may be a stacked via. The first multilevel conductive via may be a deep via. The first multilevel conductive via may be a simple-deep via. The CPS substructure may be a single CPS substructure. N may equal 2. The electrical structure may further comprise a second multilevel conductive via through the DM laminate, wherein the

second multilevel conductive via is electrically coupled to a second metal layer of the CPS substructure. The first metal layer may be at the first external surface of the CPS substructure. See FIG. 6 showing single CPS substructure 10, DM laminate 40, N=2, dielectric layers 41 and 43, metallic layers 42 and 44, first metal layer 14, stacked via 58, deep via 56, simple-deep via represented by the combination of simple via 36 and deep via 55, first multilevel conductive via 57, second multilevel conductive via 55, and the claimed structural relationships. See also description of FIG. 6 in specification, page 12, lines 2-18.

The electrical structure may further comprise a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure, wherein the first multilevel conductive via is electrically coupled to the first metal layer of the CPS substructure through the conducting via. The fraction may be less than 1, wherein the first metal layer is within an interior of the CPS substructure. The fraction may be less than 1, wherein the first metal layer is a complex power-signal of the CPS substructure. The fraction may equal to 1 such that the conducting via extends to a second external surface of the CPS substructure, wherein the first metal layer is at the second external surface. See FIG. 6 showing conducting via 36 wherein the fraction is less than 1 and conducting via 24 wherein the fraction is equal to 1. See also description of FIG. 6 in specification, page 12, lines 2-18.

The electrical structure may further comprise a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, wherein a second multilevel conductive

via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure. M may equal N. A semiconductor chip may be coupled to a metallic layer of the N metallic layers that is furthest from the CPS substructure. See FIG. 6 showing second DM laminate 39, M=2, dielectric layers 141 and 143, metallic layers 142 and 144, second metal layer 116, and second multilevel conductive via 156. See also description of FIG. 6 in specification, page 12, lines 2-18.

The electrical structure may further comprise a conductive through hole through a total thickness of the electrical structure, including through the DM laminate, the CPS substructure, and the second DM laminate. See FIG. 7 showing through hole 80; see specification, page 12, lines 1-2.

ISSUES

1. Whether claims 28-31, 33, 35-41, 51-54, 56, and 58-64 are unpatentable under 35 U.S.C. §103(a) over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955).

2. Whether claims 42-44 are unpatentable under 35 U.S.C. §103(a) over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955).

3. Whether claim 49 is unpatentable under 35 U.S.C. §103(a) over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955), and further in view of Koontz et al. (US 6,181,004).

GROUPING OF CLAIMS

The claims are grouped as shown in Table 1.

Table 1

Group	Issue	Claims	Do Claims of Group Stand or Fall Together
1	1	28, 30, 33, 35-37, 51, 53,56, 58-60	Yes
2	1	29, 52	Yes
3	1	31, 54	Yes
4	1	38-41, 61-64	Yes
5	2	42, 44	Yes
6	2	43	Yes
7	3	49	Yes

The claims of Group 2 do not stand or fall together with the claims of Group 1, because the claims of Group 2 relate to the following question/issue not relevant to the claims of Group 1: whether DiStefano in view of Noddin teaches or suggests "wherein the first multilevel conductive via is a stacked via".

The claims of Group 3 do not stand or fall together with the claims of Groups 1-2, because the claims of Group 3 relate to the following question/issue not relevant to the claims of Group 1: whether DiStefano in view of Noddin teaches or suggests "wherein the first multilevel conductive via is a simple-deep via".

The claims of Group 4 do not stand or fall together with the claims of Groups 1-3, because the claims of Group 4 relate to the following question/issue not relevant to the claims of

Groups 1-3: whether DiStefano in view of Noddin teaches or suggests "further comprising a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure".

The claims of Group 5 do not stand or fall together with the claims of Groups 1-4, because the claims of Group 4 relate to the following question/issue not relevant to the claims of Groups 1-4: whether DiStefano in view of Noddin teaches or suggests "a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure".

The claims of Group 6 do not stand or fall together with the claims of Groups 1-5, because the claims of Group 6 relate to the following question/issue not relevant to the claims of Groups 1-5: whether DiStefano in view of Noddin teaches or suggests "wherein M=N"

The claims of Group 7 do not stand or fall together with the claims of Groups 1-6, because the claims of Group 7, unlike the claims of Groups 1-6, are rejected under 35 U.S.C. §103(a) over DiStefano in view of Noddin and further in view of Koontz.

ARGUMENT

Issue 1

CLAIMS 28-31, 33, 35-41, 51-54, 56, AND 58-64 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(A) OVER DISTEFANO ET AL. (US 5,558,928) IN VIEW OF NODDIN ET AL. (US 5,276,955).

The Examiner rejected claims 28-31, 33, 35-41, 51-54, 56, and 58-64 as allegedly being unpatentable under 35 U.S.C. §103(a) over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955).

Claims 28 and 51

Appellants contend that claims 28 and 51 are not unpatentable over DiStefano in view of Noddin, because DiStefano in view of Noddin does not teach or suggest each and every feature of claims 28 and 51. For example, DiStefano in view of Noddin does not teach or suggest the following features of claim 28: "a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance" and "a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure." Similarly, DiStefano in view of Noddin does not teach or suggest the following features of claim 51: "a complex power-signal (CPS) substructure" and "a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure".

Appellants note that the Examiner has acknowledged that DiStefano does not teach or

suggest a CPS substructure. In particular, the Examiner admits: "DiStefano fails to disclose that the substructure is a complex power-signal and the first metal layer is a complex power-signal".

The Examiner argues that DiStefano discloses a DM laminate 10b and that "Noddin discloses 14 and 16 are complex power-signal and they are connected a conductor via as shown in Fig. 6 to conductive structures mounted to 18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify DiStefano by the substructure is a complex power-signal and the first metal layer is a complex power-signal, as taught by Noddin, for the purpose of providing complex power-signal to an electronic component mounted on the interposer".

Appellants view the preceding argument by the Examiner for modifying DiStefano with Noddin's allegedly disclosed CPS substructure to be unclear. First, the phrase "is a complex power-signal and the first metal layer is a complex power-signal" in unclear, since this phrase has no subject and appear to make no sense. Second, Appellants do not understand what the Examiner means by the phrase "for the purpose of providing complex power-signal to an electronic component mounted on the interposer". Appellants maintain that in the absence of a clear, understandable argument, the Examiner has not established a *prima facie* case of obviousness in relation to claims 28 and 51.

Moreover, the Examiner has not supplied a legally persuasive argument as to why a person of ordinary skill in the art would modify DiStefano by the teaching of Noddin in relation to claims 28 and 51. In particular, established case law requires that the prior art must contain some suggestion or incentive that would have motivated a person of ordinary skill in the art to modify a reference or to combine references. See Karsten Mfg. Corp. V. Cleveland Gulf Co.,

242 F.3d 1376, 58 U.S.P.Q.2d 1286, 1293 (Fed. Cir. 2001 ("In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in a way that would produce the claimed invention."). See also In re Gordon, 733 F.2d 900, 902, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984 ("The mere fact that the prior art could be so modified would not have made the motivation obvious unless the prior art suggested the desirability of the modification."). Appellant maintains that the Examiner has not made any showing of where the prior art suggests incorporation of a CPS substructure into the invention of DiStefano. By not citing any suggestion or incentive in the prior art for incorporating a CPS substructure into the invention of DiStefano, the Examiner has failed to establish a *prima facie* case of obviousness in relation to claims 28 and 51.

Appellants next present an independent analysis to demonstrate that it is not obvious to modify DiStefano by Noddin. If DiStefano discloses a DM laminate 10b as alleged by the Examiner and if Noddin discloses a CPS substructure, then Appellants assert that said CPS substructure from Noddin can only be combined with the DM laminate 10b of DiStefano if the CPS substructure is placed adjacent to DiStefano's panel 10b as required by claims 28 and 51. Claims 28 and 51 recite: "a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure". However, panel 10b is sandwiched between interposers 12a and 12c (see FIG. 1 of DiStefano). Therefore, the placement of the CPS substructure adjacent to the panel 10b would disturb the alternating pattern of circuit panels 10 and interposers 12 and thus destroy the DiStefano invention. In particular, DiStefano discloses in

col. 4, line 57 - col. 5, line 9:

> "**A method according to this aspect or the invention preferably includes the step of stacking the circuit panels and interposers in superposed relation so that each interposer is disposed between two circuit panels, with the major surfaces of the interposers and circuit panels confronting one another, and with interconnect locations on the confronting surfaces of the circuit panels and interposers being aligned with one another**. The method most preferably further includes the step of causing the flowable dielectric material to flow and conform to the major surfaces of the circuit panels. The method desirably includes the step of causing the flowable dielectric material to flow and conform to the major surfaces of the circuit panels and on the interposers into continuous electrical conductors extending between adjacent circuit boards at their respective interconnect locations. Most preferably, the flowable dielectric and flowable conductive materials are caused to flow concomitantly with one another in a single step involving application of heat and pressure to the stacked circuit panels and interposers" (emphasis added).

Appellants contend that the preceding quote from DiStefano makes it clear that the alternating pattern of circuit panels and interposers is an essential aspect of the DiStefano invention and cannot be modified. For example, it is important in DiStefano that "each interposer is disposed between two circuit panels, with the major surfaces of the interposers and circuit panels confronting one another" so that the flowable dielectric material will flow and conform to the major surfaces of the circuit panels, and so that the flowable dielectric material flows and conforms to the major surfaces of the circuit panels. This principle underlying the

DiStefano invention is repeated throughout the DiStefano disclosure and in the DiStefano claims. For example, see claim 1 of DiStefano. Thus, Appellants maintain that to add a CPS substructure within the structural configuration of DiStefano adjacent to the DM laminate 10b will disable the preceding relationship between the circuit panels and the interposers such that the DiStefano invention will be effectively destroyed.

Appellants also note that DiStefano in view of Noddin does not teach or suggest the following feature of claim 28: "a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test ". The Examiner's argument that "DiStefano discloses testing the substructures" is not persuasive, since claim 28 requires testing a CPS substructure and DiStefano does not teach or suggest a CPS substructure as admitted by the Examiner. DiStefano discloses testing only circuit panels and interposers.

Based on the preceding arguments, Appellants respectfully maintain that claims 28 and 51 are not unpatentable over DiStefano in view of Noddin, and that claims 28 and 51 are in condition for allowance. Since claims 29-31, 33, 35-41, and 63-64 depend from claim 28, Appellants contend that claims 29-31, 33, 35-41, and 63-64 are likewise in condition for allowance. Since claims 52-54, 56 and 58-62 depend from claim 51, Appellants contend that claims 52-54, 56 and 58-62 are likewise in condition for allowance.

Claims 29 and 52

Claims 29 and 52 recite: "wherein the first multilevel conductive via is a stacked via".

The Examiner's allegation that via 26b in FIG. 2 of DiStefano is a stacked via is incorrect, because Appellants' specification defines a stacked via as characterized by "discontinuities in sidewall smoothness at layer interfaces", which is not satisfied by via 26b in FIG. 2 of DiStefano. See Appellants' specification, page 8, lines 19-21.

In "Response to Arguments", the Examiner incorrectly views said discontinuities as limitations which cannot be read into the claims. Appellants maintain that a "stacked via" includes said discontinuities as a matter of definition and not as a matter of limitation. Appellants carefully defined a variety of different types of vias in the specification and these definitions are read into the claims because they are definitions rather than limitations. In the specification, the term "via" has special cases of simple via, stacked via, deep via, etc., all of which are carefully defined in the specification and such definitions apply to the claims.

Claims 31 and 54

Claims 29 and 52 recite: "wherein the first multilevel conductive via is a stacked-deep via". A simple-deep via is defined in Appellants' specification as "combination of a simple via and a deep via in electrically conductive contact". See specification, page 9, lines 11-12. Appellants contend that DiStefano does not teach or suggest a stacked-deep via. Although the Examiner alleges that DiStefano discloses a stacked-deep via, the Examiner has not provided any citation in DiStefano in support of the Examiner's allegation. Thus, the Examiner has failed to establish a *prima facie* case of obviousness in relation to claims 28 and 51.

Claims 38-41 and 61-64

Claims 38 and 61 recite: "a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure", and claims 39-41 and 62-64 recite limitations on said "fraction". On page 3, lines 3-9 of the final office action mailed 12/31/2003, the Examiner argues that DiStefano discloses the "fraction" of claims 38 and 61, wherein the Examiner's arguments relate to vias 26, 26b, and 26c of DiStefano.

In response, Appellants contend that the Examiner's arguments relating to vias 26, 26b, and 26c are irrelevant, since vias 26, 26b, and 26c are not vias of a CPS substructure as required by claims 38-41 and 61-64. As explained *supra*, the Examiner admits that DiStefano does not disclose a CPS substructure. Thus, the Examiner has failed to establish a *prima facie* case of obviousness in relation to claims 38-41 and 61-64.

Issue 2

CLAIMS 42-44 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(A) OVER DISTEFANO ET AL. (US 5,558,928) IN VIEW OF NODDIN ET AL. (US 5,276,955).

The Examiner rejected claims 42-44 as allegedly being unpatentable under 35 U.S.C. §103(a) over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955).

Appellants respectfully contend that claim 42 is not unpatentable over DiStefano in view of Noddin, because DiStefano in view of Noddin does not teach or suggest each and every feature of claim 42. For example, DiStefano in view of Noddin does not teach or suggest the following features of claim 42: "a complex power-signal (CPS) substructure that has satisfied an electrical performance acceptance test for at least one of an electrical integrity and electrical

signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance, a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a first metal layer of the CPS substructure", based on the same reasons presented *supra* in conjunction with claim 28.

In addition, DiStefano in view of Noddin does not teach or suggest "a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure".

The Examiner argues: "DiStefano/Noddin fail to disclose providing another DM laminate to the opposite side of the CPS substructure. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide another DM laminate, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8. Further, it would have been obvious to one having ordinary skill in the art at the time the invention was made to position another DM laminate to the opposite side of the CPS substructure, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ

70."

Appellants respectfully contend that the preceding argument by the Examiner is not legally persuasive, because the Examiner has inaccurately stated the holdings in *St. Regis Paper* and *In re Japikse*. In addition, the Examiner has not applied *St. Regis Paper* and *In re Japikse* to the pertinent aspects of claim 42 in accordance with acceptable standards of legal analysis. In the absence of credible legal analysis by the Examiner, the preceding argument by the Examiner is not legally persuasive. Appellants respectfully maintain that "it has been held that rearranging parts of an invention involves only routine skill in the art" is not a credible argument. Accordingly, Appellants respectfully contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 42.

In addition, "to position another DM laminate to the opposite side of the CPS substructure", as argued by the Examiner, would disturb the relationship between the circuit panels and the interposers so as to destroy the DiStefano invention, as explained *supra*.

Moreover, the Examiner has not supplied a legally persuasive argument as to why a person of ordinary skill in the art would modify DiStefano by the teaching of Noddin in relation to claim 42. In particular, established case law requires that the prior art must contain some suggestion or incentive that would have motivated a person of ordinary skill in the art to modify a reference or to combine references. See Karsten Mfg. Corp. V. Cleveland Gulf Co., 242 F.3d 1376, 58 U.S.P.Q.2d 1286, 1293 (Fed. Cir. 2001 ("In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them

in a way that would produce the claimed invention."). See also In re Gordon, 733 F.2d 900, 902, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984 ("The mere fact that the prior art could be so modified would not have made the motivation obvious unless the prior art suggested the desirability of the modification."). Appellant maintains that the Examiner has not made any showing of where the prior art suggests incorporation into the invention of DiStefano the features of: "a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure". By not citing any suggestion or incentive in the prior art for incorporating the preceding features into the invention of DiStefano, the Examiner has failed to establish a *prima facie* case of obviousness in relation to claims 28 and 51.

Based on the preceding arguments, Appellants respectfully maintain that claim 42 is not unpatentable over DiStefano in view of Noddin, and that claim 42 is in condition for allowance. Since claims 43-44 depend from claim 42, Appellants contend that claims 43-44 are likewise in condition for allowance.

Claim 43

The Examiner has not presented any argument relating to claim 43 which recites the feature: "wherein M=N". Accordingly, Appellants respectfully contend that the Examiner has

failed to establish a *prima facie* case for obviousness in relation to claim 43.

Issue 3

CLAIM 49 IS NOT UNPATENTABLE UNDER 35 U.S.C. §103(A) OVER DISTEFANO ET AL. (US 5,558,928) IN VIEW OF NODDIN ET AL. (US 5,276,955), AND FURTHER IN VIEW OF KOONTZ ET AL. (US 6,181,004).

The Examiner rejected claim 49 as allegedly being unpatentable under 35 U.S.C. §103(a) over DiStefano et al. (US 5,558,928) in view of Noddin et al. (US 5,276,955), and further in view of Koontz et al. (US 6,181,004).

Appellants respectfully contend that claim 49 is not unpatentable over DiStefano in view of Noddin, and further in view of Koontz, because DiStefano in view of Noddin, and further in view of Koontz does not teach or suggest each and every feature of claim 49. For example, DiStefano in view of Noddin, and further in view of Koontz does not teach or suggest "a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and erroneous an impedance; a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically coupled to a first metal layer of the CPS substructure", based on the same presented *supra* in conjunction with claim 28.

In addition, DiStefano in view of Noddin and further in view of Koontz does not teach or

suggest "a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure", based on the same arguments presented *supra* in conjunction with claim 42.

Moreover, the Examiner has not supplied a legally persuasive argument as to why a person of ordinary skill in the art would modify DiStefano by the teachings of Noddin and Koontz in relation to claim 49. In particular, established case law requires that the prior art must contain some suggestion or incentive that would have motivated a person of ordinary skill in the art to modify a reference or to combine references. See Karsten Mfg. Corp. V. Cleveland Gulf Co., 242 F.3d 1376, 58 U.S.P.Q.2d 1286, 1293 (Fed. Cir. 2001 ("In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in a way that would produce the claimed invention."). See also In re Gordon, 733 F.2d 900, 902, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984 ("The mere fact that the prior art could be so modified would not have made the motivation obvious unless the prior art suggested the desirability of the modification."). Appellant maintains that the Examiner has not made any showing of where the prior art suggests incorporation into the invention of DiStefano the features of: "a semiconductor chip coupled to a metallic layer of the N metallic layers that is **furthest** from the CPS substructure" (emphasis added). Regardless of whether or not it is obvious to

couple a semiconductor chip to the first DM laminate, the Examiner has not even addressed the limitation of having the semiconductor layer specifically coupled to the metallic layer that is **furthest** from the CPS substructure. By not addressing this limitation and by not citing any suggestion or incentive in the prior art for incorporating the preceding limitation into the invention of DiStefano, the Examiner has failed to establish a *prima facie* case of obviousness in relation to claim 49.

Based on the preceding arguments, Appellants respectfully maintain that claim 49 is not unpatentable over DiStefano in view of Noddin, and further in view of Koontz, and that claim 49 is in condition for allowance.

SUMMARY

In summary, Appellant respectfully requests reversal of the December 31, 2003 Office Action rejection of claims 28-31, 33, 35-44, 49, 51-54, 56 and 58-64.

Respectfully submitted,

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Title **COUPLING OF CONDUCTIVE VIAS TO COMPLEX POWER-SIGNAL SUBSTRUCTURES**

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APPENDIX - CLAIMS ON APPEAL

28. An electrical structure, comprising:

a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance;

a dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2; and

a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure.

29. The electrical structure of claim 28, wherein the first multilevel conductive via is a stacked via.

30. The electrical structure of claim 28, wherein the first multilevel conductive via is a deep via.

31. The electrical structure of claim 28, wherein the first multilevel conductive via is a simple-deep via

33. The electrical structure of claim 28, wherein the CPS substructure is a single CPS substructure.

35. The electrical structure of claim 28, wherein N=2.

36. The electrical structure of claim 28, further comprising a second multilevel conductive via through the DM laminate, wherein the second multilevel conductive via is electrically coupled to a second metal layer of the CPS substructure.

37. The electrical structure of claim 28, wherein the first metal layer is at the first external surface of the CPS substructure.

38. The electrical structure of claim 28, further comprising a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness

of the CPS substructure, and wherein the first multilevel conductive via is electrically coupled to the first metal layer of the CPS substructure through the conducting via.

39. The electrical structure of claim 38, wherein the fraction is less than 1, and wherein the first metal layer is within an interior of the CPS substructure.

40. The electrical structure of claim 38, wherein the fraction is less than 1, and wherein the first metal layer is a complex power-signal of the CPS substructure.

41. The electrical structure of claim 38, wherein the fraction is equal to 1 such that the conducting via extends to a second external surface of the CPS substructure, and wherein the first metal layer is at the second external surface.

42. An electrical structure, comprising:

a complex power-signal (CPS) substructure that has satisfied an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance;

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically

coupled to a first metal layer of the CPS substructure; and

a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure.

43. The electrical structure of claim 42, wherein M=N.

44. The electrical structure of claim 42, further comprising a conductive through hole through a total thickness of the electrical structure, including through the first DM laminate, the CPS substructure, and the second DM laminate.

49. An electrical structure, comprising:

a complex power-signal (CPS) substructure that has passed an electrical performance acceptance test for at least one of an electrical integrity and electrical signal delay, and wherein the test for electrical integrity includes a test for at least one of an electrical short, an electrical open, and an erroneous impedance;

a first dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2, and wherein a first multilevel conductive via through the first DM laminate is electrically

coupled to a first metal layer of the CPS substructure;

a second dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number M of dielectric layers and metallic layers such that a first dielectric layer of the M dielectric layers is formed on a second external surface of the CPS substructure, wherein M is at least 2, and wherein a second multilevel conductive via through the second DM laminate is electrically coupled to a second metal layer of the CPS substructure; and

a semiconductor chip coupled to a metallic layer of the N metallic layers that is furthest from the CPS substructure.

51. An electrical structure, comprising:

a complex power-signal (CPS) substructure;

a dielectric-metallic (DM) laminate that includes an alternating sequence of an equal number N of dielectric layers and metallic layers such that a first dielectric layer of the N dielectric layers is formed on a first external surface of the CPS substructure, wherein N is at least 2; and

a first multilevel conductive via through the DM laminate, wherein the first multilevel conductive via is electrically coupled to a first metal layer of the CPS substructure.

52. The electrical structure of claim 51, wherein the first multilevel conductive via is a stacked via.

53. The electrical structure of claim 51, wherein the first multilevel conductive via is a deep via.

54. The electrical structure of claim 51, wherein the first multilevel conductive via is a simple-deep via.

56. The electrical structure of claim 51, wherein the CPS substructure is a single CPS substructure.

58. The electrical structure of claim 51, wherein N=2.

59. The electrical structure of claim 51, further comprising a second multilevel conductive via through the DM laminate, wherein the second multilevel conductive via is electrically coupled to a second metal layer of the CPS substructure.

60. The electrical structure of claim 51, wherein the first metal layer is at the first external surface of the CPS substructure.

61. The electrical structure of claim 51, further comprising a conducting via beginning at the first external surface of the CPS substructure and extending through a fraction of a total thickness of the CPS substructure, and wherein the first multilevel conductive via is electrically coupled to the first metal layer of the CPS substructure through the conducting via.

62. The electrical structure of claim 51, wherein the fraction is less than 1, and wherein the first metal layer is within an interior of the CPS substructure.

63. The electrical structure of claim 38, wherein the fraction is less than 1, and wherein the first metal layer is a complex power-signal of the CPS substructure.

64. The electrical structure of claim 38, wherein the fraction is equal to 1 such that the conducting via extends to a second external surface of the CPS substructure, and wherein first metal layer is at the second external surface.